SOLID-STATE HIGH POWER RF OSCILLATOR

Dr. Aleksandr Gitsevich, Dr. Douglas Kirkpatrick, Lauren Dymond, Jr.

Fusion Lighting, Inc., 7524 Standish Place, Rockville, Maryland 20855 USA

Abstract — **A new kind of RF solid-state oscillator design is observed. The oscillator has two feedback loops, which provide a safe working condition for the power transistor at high levels of RF output power. The oscillator uses a high power LDMOS transistor, which provides output power greater than 65W and efficiency better than 65% at the operating frequency of 915 MHz. The oscillator is designed using microstrip lines and lumped components on Rogers RO3010™ substrate.**

I. Introduction

Solid-state transistor oscillator circuits are described in many articles and books [1] – [4]. Colpits, Hartley, and Clapp are well known oscillator configurations that use lumped components. These configurations are applicable up to frequencies of 400 MHz. Many authors recommend use of a small inductor or shorted low impedance line between the transistor common lead and 'ground' and an open circuited line on the transistor input for microwave oscillators. All well-known oscillator schematics are very good for low power solid-state RF and microwave oscillator designs. However, these schematics are not as effective for high power solid-state oscillators. Attempts to create solid-state power oscillators with power transistors using well-known schematics usually lead to transistor failures caused by voltage spikes associated with the feedback inductors during the start-up transition time. Given this reason, information about solid-state power oscillator development with output powers greater than 10W is not readily found in scientific publications or product literature.

Conventional solid-state RF and microwave oscillators produce relatively low output power ranging from a few milliwatts to a few hundred milliwatts. A conventional approach for getting higher RF output power uses a low power oscillator followed by multiple RF power amplifier stages. However, typical efficiency for this solution is no more than 55% and the size of the circuitry at that point becomes significant.

There are some applications for RF power sources where high output power, high efficiency, and a small footprint are very important. A RF powered electrodeless light bulb is one example of an application that could utilize a high power, high frequency and high efficiency compact power source. For example, certain electrodeless lamps described in U.S. Patent No. 6,137,237 beneficially utilize an RF power source that operates between a frequency range of 700 – 915 MHz, and which provides output power in excess of 60W, efficiency greater than 60%, and frequency instability of no more than 0.1%.

II. Oscillator Schematic

An oscillator block level schematic diagram is shown in Fig 1[5].

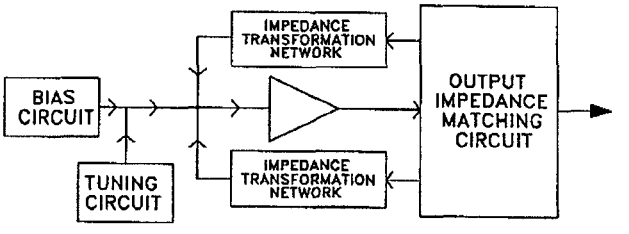

Fig. 1. Power Oscillator Block Diagram.

This oscillator design has two feedback loops. The feedback paths are created by elements of the output impedance matching circuit and the two impedance transformation networks. Each path connects the drain and gate of the transistor. The bias circuit provides the transistor gate bias, while the tuning circuit provides the ability to adjust the oscillator frequency.

The output impedance matching circuit provides matching between a 50-Ohm load impedance and the transistor drain impedance. Elements of the output impedance matching circuit and feedback impedance transformation networks provide the conditions for oscillation. These conditions are expressed by the two following relations. First, voltage gain $G_V(\omega)$ and feedback coefficient $\beta(\omega)$ must satisfy:

$$G_V(\omega)*\beta(\omega) \geq 1 \quad (1)$$

and second the phase shifts in the dual feedback loops:

$$\Sigma_i \varphi_I = 2\pi \quad (2)$$

where $\Sigma_i \varphi_I$ is the total phase shift comprised of the time delays inside the transistor, microstrip lines, and other components forming the feedback loop.

The principal oscillator schematic is shown in Fig. 2

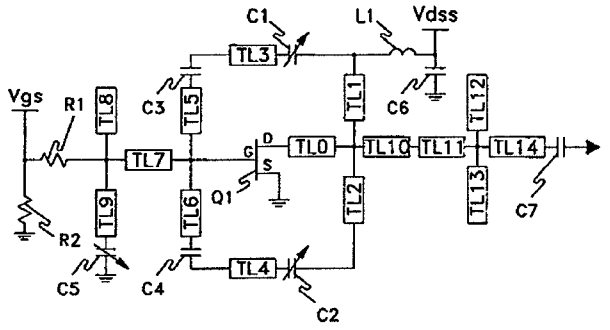

Fig. 2. Oscillator Schematic

A Motorola MRF373S transistor was used in this oscillator. The transmission lines TL0 – TL2 provide matching between the drain impedance of the transistor and the 10-Ohm line, TL10. Transmission lines TL11 – TL13 provide the transformation from 10-Ohm line impedance (TL10) to the 50-Ohm output line impedance of TL14.

Variable capacitors, C1 & C2 (0.5 - 2.5 pF), connect the opened ends of the stubs TL1 & TL2 with the feedback lines TL3 & TL4 respectively. These variable capacitors provide an adjustable feedback phase shift to help satisfy the oscillating condition in (2). Fixed capacitors C3 & C4 (both 20 pF), together with transmission lines TL5 – TL9 fulfills the feedback phase shift requirement in (2). Together these capacitors and transmission lines satisfy the amplitude oscillating condition in (1).

Lines TL8 and TL9 improves the gate match with the feedback lines. The variable capacitor C5 (0.5 - 2.5 pF) provides an adjustment of the oscillating frequency of about 50 MHz.

The two feedback loops provide an opportunity to decrease the coupling between the drain and gate networks. As a result, the RF voltage in the feedback loops is decreased, which in turn helps prevent an over volt condition leading to a breakdown on the gate due to some load mismatch (see relation (8)).

III. DESIGN FUNDAMENTALS

Choosing the right transistor is very important for obtaining a high performance power oscillator. A transistor should be selected with the following device performance characteristics in mind: 1) low saturation voltage (V_{sat}), 2) a high level of common source power gain (G_P), 3) a high value of a forward transconductance (g_m), and 4) a cutoff frequency (f_T) several times higher than the operating frequency (f).

LDMOS transistors meet these criteria and were found to be suitable for this oscillator design. Typical device characteristics for LDMOS in a power amplifier mode have a power gain (G_P) ≥ 11dB and drain efficiency $\eta \cong$ 60 %.

Recall that the MOS transistor cutoff frequency equation is:

$$f_T = g_m / 2\pi C_{GS}, \tag{3}$$

where C_{GS} is gate – source capacitance of the transistor. The amplitude and phase oscillating conditions in (1) and (2) can be transformed for our circuit into the following equations:

A. Amplitude Equation

$$\frac{2g_m R_{out}\omega\tau_{C1}\omega\tau_{C3}}{\sqrt{1+\omega^2\tau_{C1}^{\,2}}\sqrt{1+\omega^2\tau_{C3}^{\,2}}} \geq 1 \qquad \underline{2g} \tag{4}$$

In equation (4), $\tau_{C1} = C_1 Z_{fb}$. Z_{fb} is the impedance of feedback line TL3 and C_1 is the variable feedback capacitor connected to TL3. R_{out} is the real part of the transistor output impedance. $\tau_{C3} = C_3 Z_{05}$, where Z_{05} is the impedance of the line TL5 and C_3 is the fixed capacitor connecting line TL3 to line TL5.

The amplitude equation can be expressed in microwave terms:

$$S_{12}^{\,2} \cdot G_P \geq 1 \tag{5}$$

where S_{12} is the feedback transfer scattering parameter.

B. Phase Equation

$$\varphi_T + 2\pi\sum_i \frac{L_i}{\lambda_i} - \operatorname{atan}\frac{1}{\omega C_1 Z_{fb}} - \operatorname{atan}\frac{1}{\omega C_3 Z_{05}} + \operatorname{atan}\omega Z_{05} C_{GS} \cong \pi \tag{6}$$

In equation (6) the first term is the phase delay in the transistor, which can be calculated from

$$\varphi_T = 2\pi f / f_T \tag{7}$$

The second term is the sum of the phase delays in lines TL0, TL1, TL3, & TL5. Other terms are the phase shifts due to capacitors C_1, C_3, and transistors gate to source capacitance, C_{GS}.

C. Gate Protection Condition

The gate protection condition helps limit the maximum level of the RF voltage on the transistor gate to prevent breakdown. The RF voltage on the gate should be less than maximum rating of the gate - source voltage $V_{GS\,max}$ for any circumstance. An approximate condition can be expressed as:

$$2(V_{DC}-V_{sat})\frac{\omega\tau_{C1}}{\sqrt{1+(\omega\tau_{C1})^2}}\le V_{GS\max} \tag{8}$$

Matching elements between the transistor drain and 50 Ohm output line can be determined using a Smith Chart or any circuit simulation software. Nominal feedback component values and line characteristics were determined using the combination of (3) – (8) and Eagleware™ circuit simulation software.

IV. DESIGN RESULTS

The Motorola MRF373S LDMOS transistor was selected for its performance characteristics as defined in Section III. The substrate was Rogers RO3010, with ε_r=10.2 and h= 0.025 in.. The oscillator layout with surface mounted components is shown on the Fig. 3

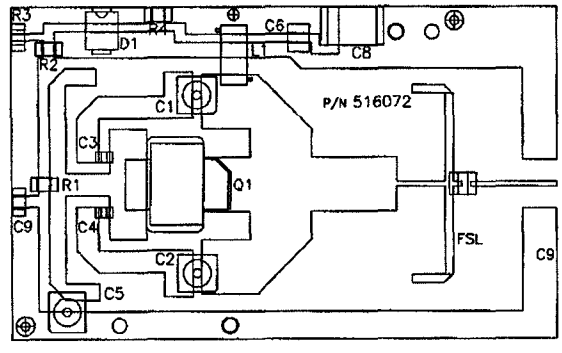

Fig. 3. Oscillator Layout with Components

The oscillator gate bias source, V_{GS}, is created by dividing the drain source voltage, V_{DSS}, through resistor R4 (3.3 KOhm), Zener diode D1(8.2 V), and resistor divider network comprised of R1 & R2 (both 4 kOhm).

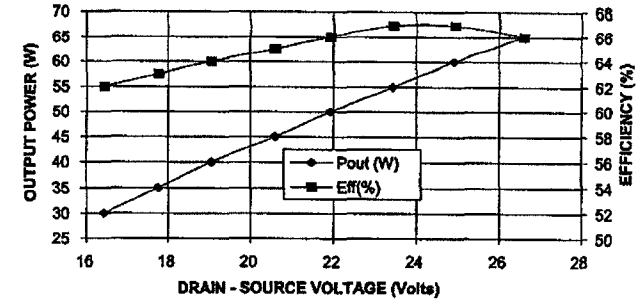

Fig. 4. Oscillator Output Power and Efficiency Vs. Drain -Source Voltage.

Figure 4 shows that the output power increases linearly with increasing drain – source voltage. A maximum power of 65W was achieved at 26.5V on the drain. Maximum efficiency was achieved for a drain-source voltage of 24V. The efficiency at maximum power (65W) was 65%. Oscillator performance measurements were made under a matched load condition into a 50-Ohm dummy load.

The change in oscillating frequency for different values of output power is shown in Fig. 5.

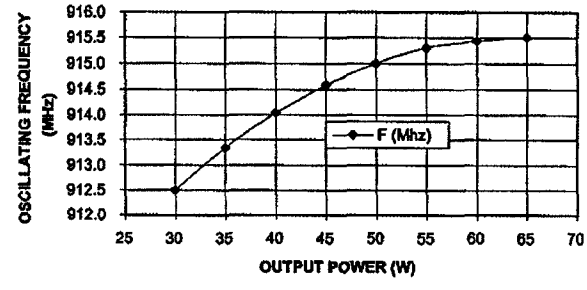

Fig. 5. Oscillating Frequency Vs. Output Power.

Figure 5 shows the oscillating frequency is sensitive to the change in drain – source voltage. By comparing Figures 4 and 5 at the maximum output power, a change of 1.5V in V_{DS} changes the oscillation frequency by 100 kHz. This correlates to a frequency/voltage sensitivity of 66kHz/V or 0.007% *f*/V at the maximum output power. This very small sensitivity can be explained by the saturation of the drain-junction capacitance given the high voltage on the drain.

The dissipated power in the transistor is 35W. Given that the junction to case thermal resistance ($R_{\theta JC}$) is 0.75°C/W, the drain junction temperature is 26.25°C over the case. The drain junction temperature is therefore

significantly less than the maximum operating junction temperature (T_J) of 200°C.

The effect of temperature of the operation of the oscillator is most readily seen during start and run-up of the oscillator. After turn on, the oscillation frequency will move 0.5 – 0.8 MHz until the oscillator temperature comes to equilibrium. This usually takes 2 to 3 minutes. The day to day variation in oscillation frequency is within 30 – 50 kHz.

The short time frequency variation (which causes phase noise) is 10 kHz. This frequency variation is not significant for the intended application of this oscillator to act as an RF power source for driving electrodeless lamps because the loaded Q of the resonant lamp system is low Q≈22 and the corresponding 3 dB BW is ≈30 MHz.

V. CONCLUSIONS

- A high Q inductor in the feedback circuit of the oscillator may cause large voltage spikes during the start-up transition time resulting in a breakdown at the gate.
- In lieu of using inductors and to prevent large voltage spikes, distributed microstrip lines can be used to limit the transition or mismatch over-voltage condition to two times the input voltage if the correct coupling feedback lines and capacitors are chosen.
- LDMOS transistors provide excellent performance for high power oscillator configurations due to high power gain, high channel conductivity, high cutoff frequency and low saturation voltage.
- This type of solid-state high power oscillator design can provide highly efficient, reliable, and robust RF power sources.

ACKNOWLEDGEMENTS

This work was supported in part by Government contract no. DE-FG01-95EE23796 awarded by the Department of Energy.

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[5] Oscillator circuitry subject to worldwide patents, International Patent Publication # WO 99/36940